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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/814,321 | 03/21/2001 | Gary F. Feierbach | ALP1P203 | 4455 |

22434 7590 12/20/2005

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| EXAMINER | |
|---|---|
| CHEN, TSE W | |
| **ART UNIT** | **PAPER NUMBER** |
| 2116 | |

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/814,321 | FEIERBACH, GARY F. | |
| | Examiner | Art Unit | |
| | Tse Chen | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8,17-25,31,32 and 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-25* is/are allowed.

6)☒ Claim(s) *1-8,31,32 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated August 3, 2005.

2. Claims 1-8, 17-25, 31-32 and 39 are presented for examination.

### *Claim Objections*

3. Claims 17 and 31 are objected to because of the following informalities:

- As per claim 17, "registering an output comprises time Tr" should be "registering an output form the functional unit comprises time Tr"; "wherein the markers are advanced through a shift register" should be "wherein the signal comprising one of a clock marker or a no-clock marker is advanced through a shift register"; "takes time Ts to advance each marker a shift register" should be "takes time Ts to advance each signal comprising one of a clock marker or a no-clock marker through a single stage of the shift register"; "a clock circuit that supplies a stage activation controller" should be "a clock circuit that supplies the stage activation controller"; "have its power status adjusted depending the requirements of the instruction entering said respective stage" should be "have its power status adjusted depending on the requirements of the instruction entering said respective stage of the functional unit".
- As per claim 31, "a stage activation controller ... to be individually activated or deactivated stage" should be "a stage activation controller ... to be individually activated or deactivated"; "whereby said AND gate controls the supply of said clock pulses to said respective" should be "whereby said AND gate controls the supply of said clock pulses to a respective stage of said functional unit".

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bartley, U.S. Patent 6219796, in view of Fletcher et al., U.S. Patent 6611920, hereinafter Fletcher.

6. In re claim 1, Bartley discloses a method for operating a microprocessor [10] to reduce power consumption [abstract], the microprocessor including a functional unit [11] formed of a plurality of stages [functional units] [col.3, ll.1-30, ll.41-65], the method comprising:

- Evaluating instructions to be executed to determine the operation type of each of said instructions, the instructions to be executed depending on operation type by said plurality of stages of said functional unit [col.4, ll.54-57; col.5, ll.1-15, ll.33-44, ll.51-57].
- Producing activity indicators [bit level machine code of either sleep or active implicit restoration instructions] by reading an operation type from an instruction and providing an associated signal [bit level machine code of either sleep or active implicit restoration instructions] based upon the operation types of said instructions [col.4, ll.54-57; col.5, ll.1-2, ll.33-44, ll.51-57; col.6, ll.8-18].
- Following said steps of evaluating said instructions and producing said activity indicators, controlling the supply of current to each of said plurality of stages such that only selected stages of said plurality of stages will draw current from a power supply, the

controlling being based upon activity indicators associated with each of said stages [col.6, ll.33-52; powering down is done after evaluating and producing steps].

- Advancing said instructions with the microprocessor [col.3, ll.16-30; operations advanced serially in stages].
- Executing said instructions that are within each of said selected stages [col.3, ll.52-61].

7. Bartley did not disclose explicitly that the stages are arranged in series or discuss the details of controlling the supply of current.

8. Fletcher discloses a method for operating a microprocessor [integrated circuit] to reduce power consumption [abstract], the microprocessor including a functional unit [FUB logic 310] formed of a plurality of stages [logical stages 310.1-310.N], where said stages of said functional unit are arranged in series [pipeline], the method comprising:

- Producing activity indicators [enable, disable] by reading an operation type from an instruction [instruction itself indicates operation type to determine enabling/disabling of clock] and providing an associated signal comprising one of a clock marker [enable] or a no-clock marker [disable] based upon the operation types of said instructions [col.3, ll.53-67].
- Following a step of producing activity indicators, controlling the supply of current to each of said plurality of stages by providing a clock signal [primary clock] and the activity indicators to a logic gate [330] that determines that only selected stages of said plurality of stages will draw current from a power supply, the controlling being based upon activity indicators associated with each of said stages [col.3, ll.53-67; col.4, ll.1-14,

ll.27-30; clock and activity indicators from scheduler control current draw following the production of activity indicators].

- Advancing the instructions within said microprocessor [col.3, ll.53-67; col.4, l.61 -- col.5, l.5].
- Executing said instructions that are within each of said selected stages [col.4, ll.27-37].

9. It would have been obvious to one of ordinary skill in the art, having the teachings of Bartley and Fletcher before him at the time the invention was made, to modify the microprocessor as taught by Bartley to include the functional unit as taught by Fletcher, in order to obtain the functional unit having the plurality of independently controlled stages arranged in series, as the pipeline series arrangement of stages is a very well known arrangement suitable for use with the microprocessor of Bartley; and providing the associated signal comprising one of a clock marker or a no-clock marker based upon the operation types of the instructions, as the utilization of clock to control the supply of current is a very well known concept suitable for use with the microprocessor of Bartley. One of ordinary skill in the art would have been motivated to make such a combination as it increases processing efficiency [via pipeline arrangement] and provides a refined way [via clock control] to decrease power consumption in a processor as the processing power increases and potential overheating is a problem [Fletcher: col.1, ll.13-32].

10. As to claim 2, Bartley discloses the microprocessor that is a very long instruction word processor [col.3, ll.41-44].

11. As to claim 3, Bartley discloses the evaluating operates to determine whether each of said instructions is an operation instruction type [active] or a no-operation instruction type [sleep] [col.5, l.51 - col.6, l.7].

12. As to claim 4, Fletcher discloses the type of instructions executed in each of said selected stages is an operation instruction type [col.4, ll.27-60].

13. As to claim 5, Bartley discloses the producing operates to produce a power-on activity indicator associated with operation instruction types [implicit], and a power-off activity indicator associated with no-operation instruction types [explicit] [col.5, l.51 - col.6, l.18].

14. As to claim 6, Fletcher discloses the selected stages are associated with power-on activity indicators, and wherein the remaining stages are associated with power-off activity indicators [col.4, l.61 -- col.5, l.13].

15. As to claim 7, Fletcher discloses the controlling operation further comprises transmitting a clock signal only to the selected stages of the functional unit [col.4, ll.10-14].

16. As to claim 8, Fletcher discloses the method further comprising repeating all of the steps for successive instructions [fig.3; pipeline architecture repeats for all instructions].

17. Claims 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bartley in view of Fletcher and Sproch et al., U.S. Patent 6247134, hereinafter Sproch.

18. In re claim 31, Bartley discloses a microprocessor [10] that operates in a manner that conserves power [abstract], the microprocessor comprising:

- An instruction evaluation unit [dispatch and decode units 11b and 11c] that evaluates a next instruction to be executed and which produces activity indicators [bit level machine code of either sleep or active instructions] [col.4, ll.54-57; col.5, ll.1-2, ll.33-44, ll.51-57].
- A functional unit [L, S, M, or D] for executing instructions [col.3, ll.1-15, ll.55-61].

19. Bartley did not discuss details relating to the functional unit.

20. Fletcher discloses a microprocessor [integrated circuit] that operates in a manner that conserves power [abstract], the microprocessor comprising:

- A functional unit [FUB logic 310] for executing instructions [col.3, ll.58-67], said functional unit having a plurality of stages [logical stages 310.1-310.N], each of said stages capable of being separately activated or deactivated based upon a respective activity indicator [enable or valid signal], where said stages of said functional unit are arranged in series [pipeline] [col.4, ll.2-5, ll.12-14].
- A stage activation controller [propagation circuit 340] that utilizes said activity indicators and causes each of said stages of said functional unit to be individually activated or deactivated, wherein said stage activation controller is a memory unit [e.g., flip flops] that stores said activity indicators [col.4, ll.17-19, ll.27-53].
- A clock circuit [primary clock; fig.3] for supplying clock pulses to each stage of said functional unit and to said stage activation controller [col.4, ll.7-14, ll.19-23].

21. It would have been obvious to one of ordinary skill in the art, having the teachings of Bartley and Fletcher before him at the time the invention was made, to modify the microprocessor as taught by Bartley to include the functional unit as taught by Fletcher, in order to obtain the functional unit having the plurality of independently controlled stages. One of ordinary skill in the art would have been motivated to make such a combination as it provides a refined way to decrease power consumption in a processor as the processing power increases and potential overheating is a problem [Fletcher: col.1, ll.13-32].

22. Furthermore, Fletcher discloses a logic gate [330.1] having an input from said stage activation controller, an input from said clock circuit and an output to one of said stages of said

functional unit, whereby said logic gate controls the supply of said clock pulses to said respective stage [fig.3; col.4, ll.6-14].

23. Fletcher discloses the logic gate as a NAND gate because the circuit was configured to operate as active low enabled [col.4, ll.19-21].

24. Sproch discloses a microprocessor [circuit 200a] that operates in a manner that conserves power [abstract], the microprocessor comprising:

- An AND gate [351] having an input [371] from the stage activation controller [propagation circuit 230a], an input [240] from the clock circuit [clk; fig.5] and an output [251] to one of the stages [register 221 or stage 231], whereby said AND gate controls the supply of the clock pulses to the respective stage [col.11, ll.7-49].

25. It would have been obvious to one with ordinary skill in the art to utilize a configuration with AND gates as taught by Sproch instead of NAND gates because Applicant has not disclosed an advantage, a particular purpose, or solution to a stated problem for using AND gates. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with configurations of other logic gates because the Applicant's invention is intended to control the activation and deactivation of the plurality of functional stages separately according to the processing of instructions, irrelevant of the logic gates that can render the same intended results.

26. As to claim 32, Fletcher discloses the memory unit is a register having a bit size equal to the number of stages in said functional unit, each bit location storing a respective activity indicator which indicates whether to activate or deactivate a respective stage [fig.3; col.4, ll.17-19].

27. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bartley and Fletcher as applied to claim 1 above, and further in view of Simonvich et al., US Patent 6308241, hereinafter Simonvich.

28. Fletcher discloses the evaluation and producing steps are performed by an instruction evaluation unit [scheduler; col.3, ll.53-67]. Fletcher and Bartley did not discuss the details of an instruction register.

29. Simonvich discloses a method comprising:

- Receiving instructions at an instruction evaluation unit [instruction cache control 118] from an instruction register [cache 114; fig.1; col.3, ll.19-23].
- Receiving instructions at a functional unit [multiplexer 128 and execution 112] from the instruction register [fig.1].

30. It would have been obvious to one with ordinary skill in the art, having the teachings of Simonvich and Fletcher before him at the time the invention was made, to modify the microprocessor as taught by Fletcher to include the configuration with the instruction evaluation and functional units receiving instructions from the instruction register as taught by Simonvich, in order to obtain more efficient processing [Simonvich: col.2, ll.24-47]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption [reduced execution cycle saves power].

***Allowable Subject Matter***

31. Claims 17-25 are allowed.

32. The following is a statement of reasons for the indication of allowable subject matter: the claims are allowable because none of the references cited, either alone or in combination

discloses or renders obvious a microprocessor of claim 17, comprising "an instruction register for temporarily storing a next instruction to be executed... an instruction evaluation unit that is connected to said instruction register... a functional unit for executing instructions... a memory unit for receiving and registering outputs from the functional unit... a stage activation controller that is connected to said instruction evaluation unit and includes logic gates... a clock circuit that supplies the stage activation controller clock pulse Csr to said stage activation controller and also provides a functional unit clock pulse Cfu to said functional unit wherein the clock pulse Cfu is subject to a gate delay of time Tg, and whrein said functional unit clock pulse Cfu is time delayed with respect to said stage activation controller clock pulse Csr by an amount of time greater than the sum of times Ts, Tr and Tg thereby enabling the respective stage of the functional unit to have its power status adjusted depending on the requirements of the instruction entering said respective stage of functional unit".

***Response to Arguments***

33. Applicant's arguments filed August 3, 2005 have been fully considered but they are not persuasive. Applicant alleges that "Fletcher and Bartley alone or in any combination, do not teach or suggest all the features of claim 1". Examiner disagrees and submits that Fletcher and Bartley combined disclose each and every limitation of the claim as discussed in the rejection of the outstanding Office Action. Applicant alleges that Fletcher "teach only NAND gates and a 'propagation circuit' without any reference or suggestion of a memory circuit". Examiner disagrees and submits that latches and flip-flops [of propagation circuit 340] are considered memories by those with ordinary skill in the art.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
December 12, 2005

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